IN THE CLAIMS

The pending claims are reproduced for the Examiner's convenience below:

59. (Previously Presented) A signal generating circuit comprising:

a first generating means for generating a first periodic signal;

a second generating means for generating a second periodic signal which is in anti-phase with the first periodic signal;

a frequency divider circuit comprising,

(i) first and second input terminals for respectively receiving the first and second periodic signals;

(ii) an even number of amplifier stages connected in series with an output of the last amplifier stage being connected to an input of the first amplifier stage, wherein each amplifier stage has an associated propagation delay and a transistor coupled between a supply terminal and a reference terminal for modulating the propagation delay through the associated amplifier stage;

(iii) means for applying said first periodic signal received at said first input terminal to a control electrode of said transistor of the or each odd amplifier stage and for applying said second periodic signal received at said second input terminal to a control electrode of said transistor of the or each even amplifier stage, to modulate the propagation delays through the associated amplifier stages about half the period of said first and second periodic signals so that when the propagation delay through the or each even amplifier stage decreases, the propagation delay through the or each odd amplifier stage increases; and

(iv) an output terminal connected to the output of said last amplifier stage for outputting a generated frequency divided signal;

wherein said first and second generating means are arranged to generate the respective first and second periodic signals as analogue periodic signals having an amplitude which causes said transistors to be not fully open or fully closed but to act as variable resistances.

60. (Previously Presented) A circuit according to claim 59, wherein there are two amplifier stages connected in series.

61. (Previously Presented) A circuit according to claim 59, comprising a plurality of said frequency divider circuits connected in series.

62. (Previously Presented) A circuit according to claim 59, wherein each amplifier stage comprises a differential amplifier.

63. (Previously Presented) A circuit according to claim 59, wherein each amplifier stage comprises connection logic circuitry which includes said transistor so that for each amplifier stage the respective one of the first and second analogue periodic signals is operable to vary the propagation delay through the connection logic circuitry.

64. (Previously Presented) A circuit according to claim 59, wherein each amplifier stage comprises an amplifier with hysteresis which includes said transistor so that for each amplifier stage the respective one of the first and second periodic signals is operable to vary the hysteresis of the respective amplifier.

65. (Previously Presented) A circuit according to claim 59, wherein said frequency divider circuit is a FET type semiconductor circuit.

66. (Previously Presented) A circuit according to claim 65, wherein said frequency divider circuit is integrated monolithically with complementary FET logic.

67. (Previously Presented) A circuit according to claim 65, wherein said frequency divider circuit is a CMOS circuit integrated monolithically with CMOS logic circuitry.

68. (Previously Presented) A circuit according to claim 65, wherein said transistor is a first transistor, and wherein the input to each amplifier stage is formed by the gate of a second transistor.

69. (Previously Presented) A circuit according to claim 68, wherein the first and second transistors are connected in series between the supply terminal and the reference terminal.

70. (Previously Presented) A circuit according to claim 59, wherein the first and second analogue periodic signals have a frequency greater than 100 MHz.

71. (Previously Presented) A circuit according to claim 59, wherein said frequency divider circuit further comprises logic means for providing dividing by ratios other than simple powers of two.

72. (Previously Presented) A circuit according to claim 59, wherein each of said amplifier stages comprises a latch circuit having two inverters connected in a memory arrangement with the output of one connected to the input of the other.

73. (Previously Presented) A circuit according to claim 72 in which each inverter comprises a p-channel transistor and a n-channel transistor, and wherein the latch circuit further comprises two pairs of n-channel transistors operable to control the state of said memory arrangement.

74. (Prevously Amended) A circuit according to claim 73, wherein the aspect ratio of the n-channel transistor of each inverter is less than the aspect ratio of the n-channel transistors in the two pairs of n-channel transistors which control the state of said memory arrangement.

75. (Previously Presented) A method of frequency division using an even number of amplifier stages connected in series, with an output of the last amplifier stage connected to an input of the first amplifier stage and each amplifier stage having a transistor coupled between a supply terminal and a reference terminal, said method comprising the steps of:

applying a first periodic signal to be frequency divided by the frequency divider circuit to a control electrode of the respective transistor of the or each odd amplifier stage; and

applying a second periodic signal which is in anti-phase with the first periodic signal to a control electrode of the respective transistor of the or each even amplifier stage,

thereby to modulate the propagation delays through the associated amplifier stages about half the period of said first and second periodic signals so that when the propagation delay through the or each even amplifier stage decreases, the propagation delay through the or each odd amplifier stage increases, to generate frequency divided signal at the output of said last amplifier stage;

wherein said applying steps apply analogue periodic signals to said control electrodes, which analogue periodic signals have an amplitude which cause said transistors to not fully open or fully close but to act as a variable resistances.

76. (Previously Presented) A method according to claim 75, wherein each amplifier stage used comprises a differential amplifier.

77. (Previously Presented) A method according to claim 75, wherein each amplifier stage used comprises an amplifier with hysteresis.

78. (Previously Presented) A method according to claim 75, wherein applying the first and second periodic signals varies the strength of connection between adjacent amplifier stages.

79. (Previously Presented) A method according to claim 77, wherein applying the first and second periodic signals varies the hysteresis of each of said amplifier stages.

80. (Previously Presented) A method according to claim 75, wherein said amplifier stages used comprise an FET type semiconductor integrated circuit.

81. (Previously Presented) A method according to claim 80, wherein said amplifier stages used comprise a CMOS integrated circuit.

82. (Previously Presented) A method according to claim 75, wherein the frequency of the input signal to be divided is greater than 100 MHz.

83. (Previously Presented) A method according to claim 75, wherein said method also uses logic circuits for providing division by ratios other than simple powers of two.

84. (Previously Presented) A radio receiver comprising:

a first generating means for generating a first periodic signal;

a second generating means for generating a second periodic signal which is in anti-phase with the first periodic signal;

a frequency divider circuit comprising,

(i) first and second input terminals for respectively receiving the first and second periodic signals;

(ii) an even number of amplifier stages connected in series with an output of the last amplifier stage being connected to an input of the first amplifier stage, wherein each amplifier stage has an associated propagation delay and a transistor coupled between a supply terminal and a reference terminal for modulating the propagation delay through the associated amplifier stage;

(iii) means for applying said first periodic signal received at said first input terminal to a control electrode of said transistor of the or each odd amplifier stage and for applying said second periodic signal received at said second input terminal to a control electrode of said transistor of the or each even amplifier stage, to modulate the propagation delays through the associated amplifier stages about half the period of said first and second periodic signals so that when the propagation delay through the or each even amplifier stage decreases, the propagation delay through the or each odd amplifier stage increases; and

(iv) an output terminal connected to the output of said last amplifier stage for outputting a generated frequency divided signal;

wherein said first and second generating means are arranged to generate the respective first and second periodic signals as analogue periodic signals having an amplitude which causes said transistors to be not fully open or fully closed but to act as variable resistances.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on May 13, 2003, and the references cited therewith.

No claims are amended, canceled, or added; as a result, claims 59-84 remain pending in this application.

' 103 Rejection of the Claims

Claims 59-70, 72-82 and 84 were rejected under 35 USC ' 103(a) as being unpatentable over Kouno (JP 60-224319), newly cited prior art in view of Schilling et al. (Electronic circuits, 1989, pages 138-151).

Claims 71 and 83 were rejected under 35 USC ' 103(a) as being unpatentable over Kouno (JP 60-224319), newly cited prior art in view of Schilling et al. (Electronic circuits, 1989, pages 138-151), and in further view of Maemura (US 5,172,400).

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.*

The *Fine* court stated that:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* (emphasis in original).

The M.P.E.P. adopts this line of reasoning, stating that

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the

prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

Applicant respectfully submits that the Office Action did not make out a *prima facie* case of obviousness for at least the reasons that follow.

The Office Action admits that "Kouno does not specify the first and second periodic signals as analogue periodic signals having an amplitude which causes said transistors to not be fully open or fully closed but to act as variable resistance as called for in independent claims 59, 75, and 84." The Office Action relies on Schilling in combination with Kouno to support the rejection under 35 USC 103 and states that Schilling teaches "that field effect transistor is a voltage controlled device."

For independent claims 59, 75 and 84 the Office Action stated "it would have been obvious to a person skilled in the art at the time of the invention was made to recognize that Kouno's frequency divider will work equally well with analog clock signals, since the field effect transistors possesses properties that is adaptable to different shape of input signals as taught by Schilling," which is a mere conclusory statement of subjective belief. The Office Action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002). Applicant respectfully submits that the Office Action has not provided objective evidence for a suggestion or motivation to combine Kouno and Schilling.

Claims 60-74, and 76-83 depend, directly or indirectly, on claims 59 and 75 respectively, and are patentable over Kouno and Schilling (and Maemura in the case of dependent claim 71 and 83) for the reasons argued above, plus the elements in the claims. If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. MPEP § 2143.03.

In addition, the Office Action maintains that certain elements are inherent in the references. Applicant respectfully disagrees because the Office Action has not established a *prima facie* case of inherency because, as recited in MPEP § 2112, "In relying upon the theory of inherency, the examiner must provide basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art," citing Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

To serve as an anticipation when a reference is silent about the asserted inherent characteristic, the gap in the reference may be filled with recourse to extrinsic evidence. But, such evidence must make clear that "the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.,* 20 USPQ2d 1746, 1749 (Fed. Cir. 1991).

Applicant respectfully submits that the Examiner has not produced extrinsic evidence to show that the following elements recited in claims 64, 70, 77, 78, 79, and 82 are necessarily present in Kuono:

- Claim 64 recites that "each amplifier stage comprises an amplifier with hysteresis. . ."
- Claim 70 recites that "the first and second analogue periodic signals have a frequency greater than 100 MHz."
- Claim 77 recites that "each amplifier stage used comprises an amplifier with hysteresis."
- Claim 78 recites that "wherein applying the first and second periodic signals varies the strength of connection between adjacent amplifier stages."
- Claim 79 recites that "the first and second periodic signals varies the hysteresis of each of said amplifier stages."
- Claim 82 recites that "the frequency of the input signal to be divided is greater than 100 MHz."

Request for Telephone Interview before Next Official Action

Applicant respectfully requests a telephone interview with the Examiner before the next Official Action is issued. The Examiner is invited to telephone Applicant's attorney ((612) 349-9592) to arrange a telephone interview.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

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By their Representatives,

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Date Nov. 13 2003

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 13th day of November, 2003.

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